

# INDIGENOUS MEMORY TECHNOLOGY MOVES FROM LAB TO FAB

Relevant for: Science & Technology | Topic: Science and Technology- developments and their applications and effects in everyday life

Testing routine : silicon wafers of 200 millimetre diameter with OTP memories undergo testing.  
| Photo Credit: [Ankit Bende and Kumar Priyadarshi, IIT Bombay](#)

IIT Bombay researchers have developed a “memory technology” that can, in principle, revolutionise Indian industry and the many applications that need semiconductor chips, such as in the defence sector, automobiles and future aspirations in cell phone manufacturing. Hard disks, flash memory, etc, are examples of memory technology. There is also another form of memory called the one-time programmable memory (OTP) where the memory is written once, stored for a lifetime, and retrieved and used many times. This finds varied uses, one of which is in correcting faulty chips that have been mass produced for specific applications.

For instance, think of a chip that helps read off the temperature. Due to a manufacturing defect, the chip may read 100 degree Celsius as 101 degree Celsius. This “offset” of 1 degree may be corrected by storing the error correction parameter in the OTP memory. This is done uniquely for each chip and once stored, the memory corrects the chip’s output for its lifetime.

“OTP memories are also used for other purposes, mainly three: chip identity, secure information storage and chip calibration for error correction,” says Udayan Ganguly, professor at IIT Bombay, who holds the patents for the invention along with A. Lele, S. Sadana and P. Kumbhare.

To store the correction value, the researchers used eight memory cells, each of which would store one “bit” (that is a value of zero or one). Each of the memory cells consist of an ultrathin silicon dioxide layer which is 10-15 atomic layers thick. This is deposited uniformly over a dinner plate–sized eight-inch silicon wafer to form millions of nanoscale capacitors. “The pristine silicon dioxide layer is insulating, passing a very low current [which in digital electronics is read as a “0”]. A nanoscale lightning is generated of 3.3 volts to blow the capacitor, leading to a short circuit that produced high current [this is a “1”],” says Prof. Ganguly. Thus, the OTP memory remembers either the “0” state or “1” state through its lifetime.

The group, in collaboration with the Semi-Conductor Laboratory, Mohali, Punjab (SCL), has successfully demonstrated CMOS 180-nanometre–based, production-ready, eight-bit memory technology, according to a press release from the office of the Principal Scientific Adviser to Government of India. Reiterating this, Prof Ganguly says, “We have shown that the memory cells and arrays pass all the specifications for the trimming application when manufactured in the SCL 180-nanometre CMOS line. These include successful operation between minus 40 degrees C to 125 degrees C and reliability to ensure excess of 95% yield on eight-bit memories.”

According to him, a large fraction of manufactured chips may need to be discarded for faults that can be corrected using this technology. This technology is the first indigenous semiconductor memory technology adoption to manufacturing at 180-nanometre node. Thus, this is a major national milestone for semiconductor innovation, says Prof Ganguly.

There exist other methods of achieving OTP memories than described above. However, these demand challenging engineering techniques and also require high voltage, which comes with a

large area penalty.

“In contrast, we use a dedicated insulator material which is specially engineered silicon dioxide at 2.5-nanometre thickness to breakdown at 3.3 volt without any special structures along with a standard transistor. Thus, the transistor is not disturbed, and no special high voltage generation is needed,” says Prof. Ganguly, pointing out the attractive features of the technology.

Semi-Conductor Lab (SCL), Punjab, is the first customer to try and use this technology for internal purposes. Apart from collaborating with SCL, the team at IIT Bombay partnered with IIT Delhi, SETS Chennai and Defence Research and Development Organization for hardware encryption.

“The concept came out of a PhD Thesis in IIT Bombay... This is the first indigenous 180-nanometre memory technology to have successfully graduated from lab to fab in 2021. It has taken six years in the process of translating research to manufacturing,” says Prof. Ganguly.

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