NEW INDIGENOUS SMART TECHNOLOGY SYSTEM CAN AUTOMATICALLY PROTECT POWER GRIDS FROM SHORT-CIRCUITS

Relevant for: Science & Technology | Topic: Indigenization of technology and developing new technology

An Indian researcher has developed a unique innovation of a prototype of a smart system that can protect power grids from short-circuits by either automatically diverting the current into a parallel shunt (external resistance to bypass maximum current) or limiting a current surge by developing high resistance in the current path.

Short-circuit situations also often occur in power distribution networks like power grids, resulting in huge current surges that can damage the power grids as they are not designed to handle the large surge current. These surges (fault current) damage the power grids causing major economic loss and disruption in the electricity supply.

In recent years a new fault current limiter technology has been developed, namely, using superconductors. These are called as superconducting fault current limiters (SCFL). This technology developed is based on the property of superconductors offering zero resistance to currents up to a threshold current value, namely, the critical current. At currents beyond the critical current, the resistance of the superconductor becomes high. Thus, the SCFL's operating principle is that when the fault current exceeds the critical current of the superconductor, its resistance becomes high. This reduces the fault current, and when the fault current reduces below the threshold critical current, the normal zero resistance mode offering operation returns. The SCFL is energy efficient in its operation. Companies in the west are already investing in superconducting fault current limiters (SCFL) technology. However, they are expensive, with an approximate cost of each superconducting fault current limiter being in the range of Euro 1 million ~ Rupees 8,00,00,000 (Eight crores).

Prof. Satyajit Banerjee from the Indian Institute of Technology Kanpur (IIT Kanpur) and his group (Md. Arif Ali) have indigenously developed a unique innovation of a prototype of a Smart Superconducting Fault Current Limiter (SCFLsm), which has a circuit wherein a superconducting element has an array of hall sensors distributed around the superconductor.

This circuit is connected in parallel to a low resistance shunt through a switch. The array of hall sensors allows continuous monitoring of current flowing through different regions of the superconductor used in the SCFLsm. Precise and continuous motoring of the current through the fault limiting superconducting element can trigger automatic action, like, diverting the current into a parallel shunt and protecting the grid. This smart aspect of the SCFLsm is that it allows for fault limiting action at any user-settable, predetermined threshold value of current flowing through the SCFLsm. This feature is unlike a conventional SCFL where fault limiting action sets in only the critical current value, which is fixed by the material of the superconductor and the processing it underwent during the synthesis of the superconductor.

Another advantage is that the SCFLsm allows for the continuous monitoring and mapping of the current distribution across the superconductor used inside it. This enables the direct visualization of any instability setting in the SCFLsm during its operation. If any instability sets in the superconductor while the SCFLsm is operating at high currents, the mapping technology will detect its development. Subsequently, corrective action can be initiated to divert the current from the superconductor and protect the SCFL. Thus the common problem of failures of the superconductors experienced in conventional SCFL's can be mitigated. The operation of this

SCFLsm is completely automatic and independent of any manual intervention for resetting the system after a fault.

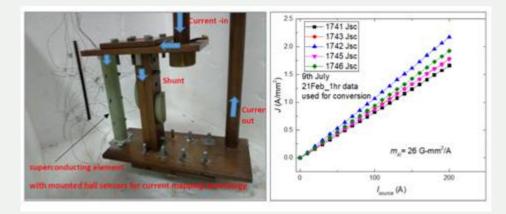
The technology developed with support from the Advanced Manufacturing Technologies Program of the Department of Science & Technology (DST), Government of India is in the 4th stage of Technology Readiness level, and a national patent has also been filed for the same. The prototype can be incorporated in any of the large power sector companies who are working with their standard superconducting fault current limiters.

Prof. Banerjee further plans to develop more efficient, large current automatic compact switches to divert current between superconductors to shunt. This will help diversion of the faulty as soon as it is detected by the smart sensors built into his SCFCLsm prototype.

He also plans to develop predictive (intelligence) capability in his smart SCFL to automatically detect when one is nearing the threshold of formation of instability in the superconducting element or even to detect when the system is approaching the stage of fault occurrence. In this situation, the system will develop smartness and have sensors that will impart it something akin to intelligence to take rudimentary decisions.

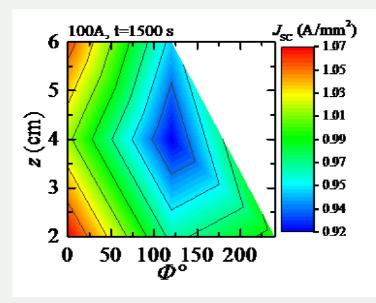


The figure above shows the fully integrated smart superconducting fault current limiter in operation.



The image on the left is an image of the actual Heart of the smart superconducting fault current limiter prototype, which has been designed, fabricated, developed, and associated electrical circuitry developed to handle multiple sensors placed around the superconductor to monitor

current. The image on the right is the measurement of current from five different hall sensors placed around the superconductor at different locations. Each sensor output is a measure of the current density J in its vicinity on the superconductor, which is being measured for different current (Isource on x-axis) being sent through the superconductor.



The image above is a map of the current distributed on the surface of the cylindrical superconductor used inside our SCFLsm prototype. The image is taken while 100 Amps of current is flowing into the superconductor. The current of 100 Amps is close to (but below) the critical current of 160 Amps of the superconductor. The color map represents the local value of the current density at a location on the superconductor surface. The map clearly shows non-uniform with patches carrying low and high current and suggests a regime of instability of operation approaching it in the superconductor.

References

Patent information: System and method for a hall sensor - superconductor based limiter of fault current, Inventors: Arif Ali and <u>Satyajit S. Banerjee</u>, Filed on: 19 March 2020. Ref. nos: 1808939IN-CS

Demonstration of a three-dimensional current mapping technique around a superconductor in a prototype of a conventional superconducting fault current limiter" by Md. Arif Ali and S. S. Banerjee (submitted and under review, 2021)

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For more details, contact Prof. Satyajit Banerjee (<u>satyajit@iitk.ac.in</u>), Dept. Of Physics, IIT Kanpur.

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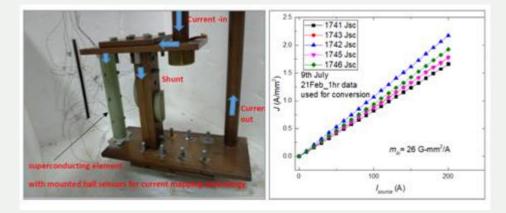
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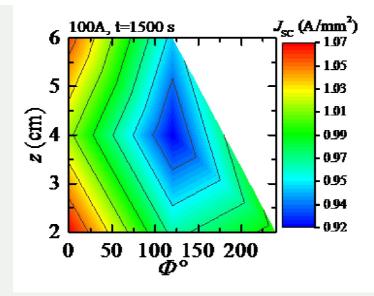
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