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THE NEED TO OVERHAUL A SEMICONDUCTOR SCHEME

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India’s $10 billion Semicon India Program has had mixed results, at best. Photo: chips-dli.gov.in

The mid-term appraisal of the semiconductor Design-Linked Incentive (DLI) scheme is due soon. Since its announcement, the DLI scheme has approved only seven start-ups, markedly short of its target of supporting 100 over five years. This impact assessment, therefore, presents an opportunity for policymakers to appraise and revamp the scheme.

India’s $10 billion Semicon India Program has had mixed results, at best. There are three goals of India’s semiconductor strategy. The first is to reduce dependence on semiconductor imports, particularly from China, and especially in strategic and emerging sectors, ranging from defence applications to Artificial Intelligence development. The second is to build supply chain resilience by integrating into the semiconductor global value chain (GVC). The third is to double down on India’s comparative advantage: India already plays host to the design houses of every major global semiconductor industry player and Indian chip design engineers are an indispensable part of the semiconductor GVC.

These goals will help cement India’s status as a semiconductor powerhouse. However, resources are limited. Therefore, priorities for industrial policy should ensure that we reap disproportionate benefits from our investments. Stimulating the design ecosystem is less capital-intensive than the foundry and assembly stages of the semiconductor GVC. Bolstering this stage can help establish strong forward linkages to an up-and-coming fabrication and assembly industry in India. Therefore, it is odd to note a concerted lack of policy scrutiny of the DLI scheme’s lack of results, while Production-Linked Incentive schemes for foundries and assembly stages received quick revisions post notification.

Prima facie, the DLI scheme fares well with its focus on providing access to design infrastructure, such as electronic design automation (EDA) tools, alongside financial subsidies for different steps of the chip design process. But there has been lacklustre uptake of the scheme. First, the scheme mandates that beneficiary start-ups maintain their domestic status for at least three years after receiving incentives, and for this they cannot raise more than 50% of their requisite capital via foreign direct investment. This is a significant barrier.

Costs for semiconductor design startups are also significant. Semiconductor R&D usually only pays off in the longer term, and the funding landscape for chip start-ups in India continues to be

challenging despite promising IP and business potential. Such capital requirements, combined with the lack of success stories caused by the absence of a mature start-up funding ecosystem for hardware products in India, reduce the risk appetite of domestic investors. Consequently, any shortfall in investment for DLI beneficiary start-ups could be bridged by equity financing bringing in foreign funds, if not for the scheme's riders on ownership.

The relatively modest incentives under the DLI scheme (capped at 15 Crore for Product DLI and 30 Crore for Deployment Linked Incentive, per application) would not make for a worthwhile trade-off for start-ups standing to lose out on access to crucial long-term funding. It is therefore crucial to delink ownership from the development of semiconductor design and adopt more start-up-friendly investment guidelines. This would also boost their financial stability and provide them global exposure.

The primary aim of the DLI scheme should be to cultivate semiconductor design capabilities in India, with the understanding that home-grown IP will organically evolve as local talent fosters the creation of indigenous companies over time. The scheme needs to be revised to focus on the broader objective of facilitating design capabilities for a wide array of chips within the country, so long as the entity engaging in the design development process is registered in India. The Union government's recent statement, that "(the product) should be an India-designed chip", implies a move in this direction. The financial outlay of the scheme must be enhanced substantially to support this policy shift.

The Centre for Development of Advanced Computing's role as the nodal agency appraising proposals by applicants under the DLI scheme merits a re-look too. As it is also a market player in the Indian chip design sector, clear concerns of a conflict of interest arise, as well as its capacity and suitability to be the implementing and regulating agency. The Karnataka government's Semiconductor Fabless Accelerator Lab (SFAL), with its specific partnerships with the Indian Electronics and Semiconductor Association, EDA vendors, IP, and testing companies, could be an appropriate blueprint for an implementing agency for DLI.

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A similar agency under the auspices of the India Semiconductor Mission could aim to emulate SFAL's approach and provide affiliated start-ups access to a network of mentors, industry, and financial institutions, in addition to the disbursal of financial incentives under the scheme. It could inspire an expanded focus for a revamped DLI scheme attracting a broader range of semiconductor design start-ups (not just ones ready for volume production) and help them overcome initial hurdles in developing design ideas. A recalibrated policy focused on chip design steered by a capable institution can tolerate a certain failure rate and treat beneficiary start-ups as exploratory risk-taking vehicles to establish India's foothold in this high-tech sector.

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