

INDIA LAUNCHES DIGITAL INDIA RISC-V (DIR-V) PROGRAM FOR NEXT GENERATION MICROPROCESSORS TO ACHIEVE COMMERCIAL SILICON & DESIGN WINS BY DECEMBER'2023

Relevant for: Science & Technology | Topic: Indigenization of technology and developing new technology

Ministry of Electronics & IT



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India through MeitY set to take Premiere Board Membership of RISC-V International to collaborate, contribute and advocate India's expertise with the RISC-V leaders of the world

Posted On: 27 APR 2022 6:09PM by PIB Delhi

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While setting the aggressive milestones for commercial silicon of SHAKTI & VEGA and their design wins by December 2023, Shri Rajeev Chandrasekhar mentioned that DIR-V will see partnerships between Startups, Academia & Multinationals, to make India not only a RISC-V Talent Hub for the World but also supplier of RISC-V SoC (System on Chips) for Servers, Mobile devices, Automotive, IoT & Microcontrollers across the globe.

Reminiscing his early days as x-86 processor chip designer at Intel, Shri Rajeev Chandrasekhar mentioned that many new processor architectures have gone through an initial period of ferment characterized by waves of innovations. At some point, however, they all settled on a dominant design. ARM and x-86 are two such instruction set architectures- one of which is licensed and other is sold, where industry consolidated in earlier decades. However, RISC-V has emerged as a strong alternative to them in last decade, having no licensing encumbrances, enabling its adoption by one and all in semiconductor industry, at different complexity levels for various design purposes.

Challenging the status quo, RISC-V Instruction Set Architecture (ISA) is not only witnessing a quantum leap and unprecedented levels of processor innovation owing to its free and open nature but also pushing the Moore's Law beyond its limits. Today, there is a thriving ecosystem of chip designers at academia, scientific societies and startups in the country, contending to gain the market share in RISC-V growing market. While India has certainly taken several early steps in processor design area, the time is felicitous now to advocate India's strides in RISC-V global community and unveil the Digital India RISC-V Processor roadmap to the world.

India today announces its ambitious roadmap with Ministry of Electronics and IT planning to join the RISC-V International as Premiere Board Member to collaborate, contribute and advocate India's expertise with other global RISC-V leaders.

Shri Rajeev Chandrasekhar while announcing the DIR-V Program with Prof. V. Kamakoti, Director, IIT Madras as Chief Architect and Shri S. Krishnakumar Rao as Program Manager. He also unveiled not only the Blueprint of the roadmap of design & implementation of the DIR-V Program with – SHAKTI Processor by IIT Madras and VEGA Processor by C-DAC but also the strategic Roadmap for India's Semiconductor Design & Innovation to catalyze the semiconductor ecosystem in the country.

RISC-V ISA, being available in Open-Source, Dr. Rajendra Kumar, Additional Secretary and Shri Arvind Kumar, Group Coordinator (R&D in Electronics), MeitY projected its growth potential and mentioned that RISC-V will pave the way for next decade of computing design and innovations and adoption in future-generation of processors.

Mr. Bob Brennan, VP, Intel Foundry Services, while speaking about the IFS (Intel Foundry Services) Innovation Fund announced by Intel to support early-stage startups and established companies building disruptive technologies for the foundry ecosystem, appreciated the Indian RISC-V movement.

Prof. V. Kamakoti, while highlighting the Intel's support for getting fabricated 22nm SHAKTI Chip at Intel foundry, mentioned that DIR-V Program will catalyze the design innovation in the country and will encourage the several domestic startups working in RISC-V domains like- micro architecture design, verification and security aspects.

Mr. Naveed Sherwani, Chairman, RapidSilicon was of the view that with India joining the RISC-V International, the Global Open Source Hardware revolution will get a new leap forward.

Ms Calista Redmond, CEO, RISC-V International highlighted the profound technical collaboration in RISC-V community by IIT Madras, one of five honored RISC-V Development partners. She also congratulated C-DAC for designing a range of RISC-V

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